



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) Publication number:

0 599 317 A1

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: **93119027.6**

(51) Int. Cl.⁵: **H01L 21/90, H01L 21/3105**

(22) Date of filing: **25.11.93**

(30) Priority: **26.11.92 JP 317005/92**

(43) Date of publication of application:
01.06.94 Bulletin 94/22

(84) Designated Contracting States:
DE FR GB IT NL

(71) Applicant: **NEC CORPORATION**
7-1, Shiba 5-chome
Minato-ku
Tokyo 108-01(JP)

(72) Inventor: **Murao, Yukinobu**
c/o NEC Corporation,
7-1, Shiba 5-chome
Minato-ku, Tokyo(JP)

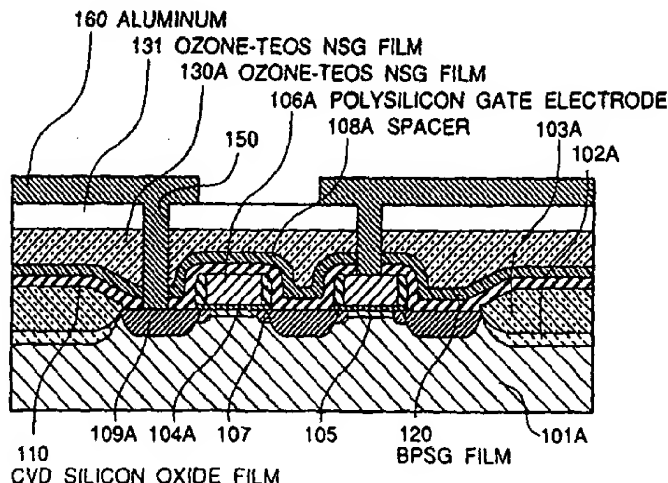
(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
D-80058 München (DE)

(54) **Planarized interlayer insulating film formed of stacked BPSG film and ozone-teos NSG film in semiconductor device, and method for forming the same.**

(57) A semiconductor device formed at a substrate surface region is coated with a non-doped CVD silicon oxide film (110), and an planarized interlayer insulating film composed of a BPSG film (120), a first ozone-TEOS NSG film (130A) and a second ozone-TEOS NSG film (131) is formed on the silicon oxide film (110). The BPSG film (120) has a thickness of not less than 50 nm but not greater than 200

nm, and is heat-treated at a temperature of not lower than 700°C but not higher than 800°C. In addition, the first and second zone-TEOS NSG films (130A,131) are also heat-treated at a temperature of not lower than 700°C but not higher than 800°C. After the heat treatment the first ozone-TEOS NSG film (130) is planarized by the etch-back of a dummy layer (140) (e.g. SOG).

FIGURE 3D



EP 0 599 317 A1

Background of the Invention

Field of the invention

The present invention relates to a semiconductor device and a method for manufacturing the same. More specifically, the present invention relates to an interlayer insulating film formed between a lower level wiring conductor layer formed of a refractory conductor material and an upper level wiring conductor formed of an aluminum type metal film.

Description of related art

In a conventional semiconductor device, such as a MOS semiconductor device, having an upper level wiring conductor formed of an aluminum type metal film, an interlayer insulating film formed of a BPSG (borophosphosilicate glass) film has been widely used. For example, this MOS semiconductor device has been essentially manufactured as follows: A semiconductor device having a diffusion layer and a polysilicon wiring conductor at a silicon substrate surface is formed, and a non-doped insulating film is formed on a whole surface of the substrate. Thereafter, a BPSG film is formed on a whole surface of the non-doped insulating film. The non-doped insulating film is provided for the purpose of preventing phosphorus or boron contained in the BPSG film from being diffused into the diffused layer. The BPSG film is reflowed by a heat-treatment for example in a nitrogen or steam atmosphere at a temperature on the order of 900°C, so that the surface is smoothed. In order to reflow the BPSG film, a temperature of not less than 850°C is required. An opening is formed through the BPSG film and the non-doped insulating film, and an upper level wiring conductor composed of an aluminum type metal film is formed. A main reason for adopting the BPSG film as the interlayer insulating film lies on a gettering property and on a reflow property.

With advanced microminiaturization of semiconductor devices, a problem occurs in connection with the reflow of the BPSG film in the case that the interlayer insulating film is formed of only the BPSG film.

Now, referring to Figures 1A and 1B which are sectional views of a semiconductor device, and to Figure 2 which is a graph showing a step coverage of the BPSG film, explanation will be made on the fact that when a BPSG film is deposited, a void occurs dependently upon the step coverage of the BPSG film.

Firstly, as shown in Figure 1A, a silicon oxide film 211A is formed on a P-type silicon substrate 201A, and a polysilicon gate electrode 206A is

formed on the silicon oxide film 211A. Then, a BPSG film 220 of a thickness "b" is formed on the whole surface. This case will be now examined. The concentration of each of phosphorus and boron contained in this BPSG film 220 is 5 mol%. Here, it is assumed that a minimum thickness of the BPSG film formed on a side surface of the polysilicon gate electrode 206A is "a". In this case, a factor "a/b" is a parameter showing the step coverage, and the dependency of the parameter "a/b" upon the thickness "b" of the BPSG film 220 is as shown in Figure 2. Namely, if the thickness "b" of the BPSG film 220 is not larger than 200 nm, the step coverage of the as-deposited film is very excellent, but if the thickness "b" of the BPSG film 220 is larger than 200 nm, the step coverage of the as-deposited film becomes bad. However, if the thickness "b" of the BPSG film 220 is not larger than 200 nm, a stray capacitance formed between the polysilicon gate electrode and the upper level wiring conductor composed of aluminum type metal film becomes large. This is not preferable.

Next, the case that the thickness "b" of the BPSG film 220 is larger than 200 nm, will be examined. As shown in Figure 2B, a silicon oxide film 211B is formed on a P-type silicon substrate 201B, and a plurality of polysilicon gate electrodes 206B are formed on the silicon oxide film 211B with intervals of 0.5 μm. Then, a BPSG film 221 having a thickness of for example 250 nm is formed on the whole surface. The concentrations of phosphorus and boron contained in the BPSG film 221 are the same as those of the phosphorus and the boron contained in the BPSG film 220, respectively. In this case, if the step coverage is excellent, the surface of the as-deposited BPSG film 221 should be substantially planar. Actually, however, voids 215 occur in the as-deposited BPSG film 211, as will be readily understood from the result shown in Figure 2.

These void 215 will disappear when the BPSG film 211 is reflowed. For this reflow treatment, a temperature of not less than 850°C is required as mentioned hereinbefore. However, if the heat-treatment is performed at a temperature of not less than 800°C, a depth of junction will increase in source/drain regions of a MOS transistor, with the result that a so-called short channel effect becomes large. This phenomenon is remarkable, particularly in a P-channel MOS transistor. Because of this reason, the interlayer insulating film formed of the reflowed BPSG film is not suitable in a semiconductor integrated circuit including micro-miniaturized semiconductor devices.

Recently, as an insulating film having an excellent step coverage, attention is focused on a non-doped silicon oxide film formed by a chemical

vapor deposition process using ozone (O_3) and tetraethoxysilane ($Si(OC_2H_5)_4$, called "TEOS" hereinafter). This non-doped silicon oxide film will be called an "ozone-TEOS NSG film" hereinafter. Here, "NSG" is an abbreviation of a "non-doped silicate glass".

However, if the interlayer insulating film is formed of only the ozone-TEOS NSG film, other problems will occur. One of the other problems is that the ozone-TEOS NSG film itself has no gettering function. In addition, the as-deposited ozone-TEOS NSG film has a high moisture content, and therefore, a heat-treatment is required. During the heat-treatment, however, the moisture moves to the semiconductor devices. Therefore, if the interlayer insulating film is formed of only the ozone-TEOS NSG film, an electrical characteristics of the semiconductor devices is deteriorated.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a semiconductor device and a method for manufacturing the same, which have overcome the above mentioned defect of the conventional one.

Another object of the present invention is to provide an interlayer insulating film which has a gettering function and an excellently planarized surface and which never deteriorates the electrical characteristics of semiconductor devices, in a semiconductor integrated circuit including micro-miniaturized semiconductor devices, and a method for manufacturing such an interlayer insulating film.

The above and other objects of the present invention are achieved in accordance with the present invention by a semiconductor device having at least a diffusion layer and a polysilicon wiring conductor formed at a silicon substrate surface, a lower level wiring conductor layer including at least the diffusion layer, wherein the improvement is that an interlayer insulating film between the lower level wiring conductor layer and an upper level wiring conductor includes an interlayer insulating film having a planarized surface, which includes at least a BPSG film and a non-doped silicon oxide film deposited on the BPSG film by a chemical vapor deposition process using ozone and tetraethoxysilane.

Preferably, the BPSG film has a thickness of not less than 50 nm but not greater than 200 nm.

According to another aspect of the present invention, there is provided a method for manufacturing a semiconductor device, comprising the steps: forming a semiconductor device having a diffusion layer and a polysilicon wiring conductor at a silicon substrate surface, and forming a non-doped insulating film on a whole surface of the

substrate; forming, on the non-doped insulating film, a BPSG film having a thickness of not less than 50 nm but not greater than 200 nm, and then, performing a first heat-treatment; forming, on the BPSG film, a non-doped silicon oxide film by a chemical vapor deposition process using ozone and tetraethoxysilane, and then; performing a second heat-treatment; forming an insulative dummy layer on a surface of the non-doped silicon oxide film, and then, performing an etching-back treatment until the insulative dummy layer is completely removed, so that a surface of the non-doped silicon oxide film is planarized; forming openings through the BPSG film and the non-doped silicon oxide film so as to reach the diffusion layer and the polysilicon wiring conductor, respectively; and forming an upper level wiring conductor formed of an aluminum type metal film on the planarized non-doped silicon oxide film, in contact with the diffusion layer and the polysilicon wiring conductor through the openings, respectively.

Preferably, each of the first and second heat-treatments is performed at a temperature of not lower than 700 °C but not higher than 800 °C.

The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention with reference to the accompanying drawings.

Brief Description of the Drawings

Figures 1A and 1B are sectional views for illustrating the problem of the conventional semiconductor device;

Figure 2 is a graph showing the step coverage of the BPSG film, for illustrating the problem of the conventional semiconductor device;

Figures 3A to 3D are sectional views for illustrating the manufacturing process of the first embodiment of the present invention;

Figures 4A and 4B are of sectional views for illustrating the advantage of the first embodiment of the present invention;

Figure 5 is a graph showing the change of the moisture content ratio of the ozone-TEOS NSG film dependent upon the heat-treatment temperature, for illustrating the first embodiment of the present invention;

Figure 6 is a graph showing the dependency of the threshold voltage V_{TH} of the N-channel MOS transistor upon the gate length L , for illustrating the first embodiment of the present invention; and

Figure 7 is a sectional view for illustrating the second embodiment of the present invention.

Description of the Preferred embodiments

Now, the present invention will be described with reference to the drawings.

Referring to Figures 3A to 3D illustrating the manufacturing process of the semiconductor device, a first embodiment of the present invention will be formed as follows:

As shown in Figure 3A, on a principal surface of a P-type silicon substrate 101A having a specific resistance on the order of $1 \Omega \cdot \text{cm}$, there is formed a device isolation region composed of a P-type channel stopper 102A and a field oxide film 103A having a thickness on the order of 500 nm. In a device formation region defined or surrounded by the device isolation region, a gate oxide film 104A having a thickness on the order of 15 nm is formed on the principal surface of the silicon substrate 101A. In addition, a channel doped layer 105 is also formed by ion-implanting boron at the dose on the order of $3 \times 10^{12} \text{ cm}^{-2}$ to the principal surface of the silicon substrate 101A. An opening (not shown) is formed at predetermined positions of the gate oxide film 104A.

Next, an N^+ polysilicon film having a thickness on the order of 300 nm is formed on the whole surface of the substrate, and then, patterned by a conventional photolithography and dry etching so as to form polysilicon gate electrodes 106A having a gate length ($= L$) of 0.4 μm . Thereafter, by using the gate electrodes 106A as a mask, phosphorus is ion-implanted at the dose on the order of $1 \times 10^{13} \text{ cm}^{-2}$ with an acceleration energy on the order of 30 KeV, so as to form an N^- diffusion layer 107 at the principal surface of the P-type silicon substrate 101A. Furthermore, a non-doped CVD silicon oxide film 108 having a thickness on the order of 150 nm is formed on the whole surface at a deposition temperature of 800 °C (Figure 3A).

Then, the CVD silicon oxide film 108 is etched back by an anisotropic dry etching, so that a spacer 108A formed of the CVD silicon oxide film 108 is formed on each side surface of the polysilicon gate electrodes 106A, as shown in Figure 3B. In addition, by using the gate electrodes 106A having each side surface coated with the spacer 108A as a mask, arsenic is ion-implanted at the dose on the order of $5 \times 10^{15} \text{ cm}^{-2}$ with an acceleration energy on the order of 30 KeV, so as to form an N^+ diffusion layer 109A at the principal surface of the P-type silicon substrate 101A.

Furthermore, a non-doped CVD silicon oxide substrate 110 having a thickness on the order of 50 nm is formed on the whole surface. This CVD silicon oxide film 110 is provided to prevent phosphorus or boron from being diffused from a BPSG film formed in a next step, into the silicon substrate 101 or the N^- diffusion layer 107 and the N^+

diffusion layer 109A.

Thereafter, a BPSG film 120 having a thickness on the order of 100 nm is formed by a CVD process. In this BPSG film 120, the concentration of boron is about 5 mol% and the concentration of phosphorus is about 5 mol%. The thickness of this BPSG film 120 is preferably not less than 50 nm but not greater than 200 nm.

The upper limit of the thickness of the BPSG film 120 is attributable to the following: As shown in Figure 2, if the film thickness is not greater than 200 nm, the step coverage of the BPSG film is very excellent, but if the film thickness is greater than 200 nm, the step coverage of the BPSG film becomes bad. On the other hand, the lower limit of the thickness of the BPSG film 120 is attributable to the following: The BPSG film 120 getters external impurities such as sodium, so that the BPSG film 120 functions as a passivation film for protecting the semiconductor device. The BPSG film is required to have the thickness of at least 50 nm in order to function as the passivation film.

Then, a first heat-treatment is performed on this BPSG film 120 at a temperature of not lower than 700 °C but not higher than 800 °C. The reason for performing the heat-treatment at a temperature of not higher than 800 °C is to prevent increase of the depth of junction in the N^+ diffusion layer 109A. With this feature, it is possible to suppress increase of a short-channel effect of, for example, a MOS transistor. In addition, the reason for performing the heat-treatment at a temperature of not less than 700 °C is to remove moisture contained in the as-deposited BPSG film. This first heat-treatment is not for the purpose of reflowing the BPSG film.

Next, an ozone-TEOS NSG film 130 is formed on the whole surface by a chemical vapor deposition process (atmospheric pressure CVD) at a temperature of 400 °C, using ozone (O_3) and TEOS ($\text{Si}(\text{OC}_2\text{H}_5)_4$). The flow rate of {ozone : TEOS} is 10 : 1. A planar property of the as-deposited ozone-TEOS NSG film 130 will be discussed hereinafter. Succeedingly, a second heat-treatment is performed at a temperature of not lower than 700 °C but not higher than 800 °C. The temperature range of this second heat-treatment will be also discussed hereinafter.

Thereafter, an SOG film (spin on glass) 140 is coated on the whole surface. This SOG film 140 has a thickness on the order of 300 nm at its thickest portion. The SOG film 140 is baked at a temperature of 100 °C, and thereafter, a heat-treatment is performed in a nitrogen (N_2) atmosphere at a temperature of 400 °C (Figure 3B).

Then, an etching-back treatment is performed until the SOG film 140 is completely removed. With this treatment, the ozone-TEOS NSG film 130 becomes a ozone-TEOS NSG film 130a having a

planarized surface, as shown in Figure 3C. Here, in place of the SOG film 140, a photoresist film can be formed on the ozone-TEOS NSG film 130, and then, an etching-back treatment can be performed.

Here, openings may be formed at a predetermined position to reach the polysilicon gate electrode 106A and at another predetermined position to reach the N^+ diffusion layer 109A, respectively. However, the surface of the ozone-TEOS NSG film 130a has minute convexities and concaves because of the etching-back treatment. Therefore, it is more preferable to relax or smoothen the minute convexities and concaves. For this purpose, another ozone-TEOS NSG film 131 having a thickness on the order of 20 nm is formed on the whole surface. This ozone-TEOS NSG film 131 has a planar surface in an as-deposited condition. Succeedingly, a heat-treatment is performed under the same condition as that of the above mentioned second heat-treatment. Thus, an interlayer insulating film formed of the BPSG film 120, the ozone-TEOS NSG film 130 and the ozone-TEOS NSG film 131 which are deposited and stacked in the named order, is completed as shown in Figure 3D. Here, in place of the ozone-TEOS NSG film 131, a BPSG film can be formed and a heat-treatment is performed under the same condition as that of the above mentioned first heat-treatment. Alternatively, a SOG film can be coated and baked, in place of the ozone-TEOS NSG film 131.

Thereafter, openings 150 are formed at a predetermined position to reach the polysilicon gate electrode 106A and at another predetermined position to reach the N^+ diffusion layer 109A, respectively. In addition, an upper level wiring conductor 160 formed of an aluminum type metal film is formed. Thus, a semiconductor device is completed.

Now, the planar property of the ozone-TEOS NSG film in the first embodiment will be explained with reference to Figures 4A and 4B which are sectional views of a semiconductor device.

As shown in Figure 4A, a silicon oxide film 111AA is formed on a P-type silicon substrate 101AA, and one polysilicon gate 106AA is formed on the silicon oxide film 111AA. Next, an ozone-TEOS NSG film 132 having a thickness on the order of 800 nm, which is sufficiently larger than the thickness of the BPSG film, is formed on the whole surface. Although this ozone-TEOS NSG film 132 has a large thickness, this ozone-TEOS NSG film 132 has an excellent step coverage in an as-deposited condition, differently from the BPSG film as shown in Figure 1A. Therefore, even in the case that a silicon oxide film 111AB is formed on a P-type silicon substrate 101AB, and a plurality of polysilicon gates 106AB are formed on the silicon oxide film 111AB with intervals of 0.5 μm , and

then, an ozone-TEOS NSG film 133 having a thickness of for example 800 nm is formed on the whole surface as shown in Figure 4B, voids (which occurred in the BPSG film) do not occur. The as-deposited film has an excellent step coverage.

Here, a supplementary explanation will be made on the limitation of the temperature in the second heat-treatment in the first embodiment. Since a reaction product of the chemical vapor deposition process using the ozone (O_3) and the TEOS ($\text{Si}(\text{OC}_2\text{H}_5)_4$) includes moisture (H_2O), the as-deposited ozone-TEOS NSG film has a high moisture content as mentioned hereinbefore. Accordingly, the heat-treatment becomes necessary. Referring to Figure 5 showing a change of the moisture content ratio of the ozone-TEOS NSG film dependent upon a heat-treatment temperature (ratio of the moisture content of the heat-treated film to the moisture content of the as-deposited film deposited at 400°C), it will be noted that it is necessary to perform the heat-treatment at a temperature of not lower than 700°C (the BPSG film has a similar inclination). The graph of Figure 5 was obtained by measuring an infrared absorptivity of OH group. In addition, the second heat-treatment at a temperature of not higher than 800°C is intended to prevent increase of the depth of junction in the N^+ diffusion layer 109A and others, similarly to the upper limit of the temperature of the first heat-treatment.

Referring to Figure 6 which is a graph showing the threshold voltage V_{TH} of an N-channel MOS transistor dependent upon a gate length L, if the gate length L is not smaller than 0.4 μm in the N-channel MOS transistor of the above mentioned first embodiment, the short-channel effect is not remarkable. In the prior art, on the other hand, the gate length L of not smaller than 0.7 μm is required in order to suppress the short-channel effect.

Referring to Figure 7 which is a sectional view of a semiconductor device, a second embodiment of the present invention is such that a lower level wiring conductor layer is composed of an N^+ diffusion layer 109B, a polysilicon gate electrode 106B formed of N^+ polysilicon film, and a silicide wiring conductor 114. In a surface of a P-type silicon substrate 101B, there are formed a device isolation region composed of a P-type channel stopper 102B and a field oxide film 103B, and a gate oxide film 104. The polysilicon gate electrode 106B is formed on the gate oxide film 104B. The polysilicon gate electrode 106B, the gate oxide film 104B and the field oxide film 103B are coated with a non-doped first interlayer insulating film 112. The silicide wiring conductor 114 is connected to the N^+ diffusion layer 109A through an opening 113 formed in the first interlayer insulating film 112. A

second interlayer insulating film between the silicide wiring conductor 114 and an upper level wiring conductor (not shown) of an aluminum type metal film is formed by depositing a BPSG film 121, an ozone-TEOS NSG film 134 having a planarized surface, and another BPSG film 122 in the named order. The conditions for forming the BPSG film 121 and the ozone-TEOS NSG film 134 are the same as those for forming the BPSG film 120 and the ozone-TEOS NSG film 130 in the first embodiment, respectively.

In the above mentioned second embodiment, it is possible that the BPSG film 121 is in direct contact with a lower level wiring conductor, such as the silicide wiring conductor 114, which has no problem in connection with diffusion of conductive impurities. Therefore, the planar property of the surface of the second interlayer insulating film can be maintained. In addition, even if the lower level wiring conductor layer composed of a refractor conductor material includes a plurality of lower level wiring conductor layers having no problem in connection with diffusion of conductive impurities this embodiment can be applied.

As mentioned above, the present invention is characterized in that an interlayer insulating film between a lower level wiring conductor layer formed of a refractory conductor material and all upper level wiring conductor formed of an aluminum type metal film, includes an interlayer insulating film having a planarized surface, which includes at least a BPSG film and an ozone-TEOS NSG film deposited on the BPSG film. Therefore, the reflow of the BPSG film becomes unnecessary, and therefore, the restriction on microminiaturization of the semiconductor device is reduced. In addition, since the BPSG film has a gettering function, although the ozone-TEOS NSG film is included in the interlayer insulating film, the deterioration of the electrical characteristics of the semiconductor device can be avoided.

The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the present invention is in no way limited to the details of the illustrated structures but changes and modifications may be made within the scope of the appended claims.

Claims

1. A semiconductor device having at least a diffusion layer and a polysilicon wiring conductor formed at a silicon substrate surface, a lower level wiring conductor layer including at least said diffusion layer wherein the improvement is that an interlayer insulating film between said lower level wiring conductor layer and an

upper level wiring conductor includes an interlayer insulating film having a planarized surface, which includes at least a BPSG film and a non-doped silicon oxide film deposited on said BPSG film by a chemical vapor deposition process using ozone and tetraethoxysilane.

2. A semiconductor device claimed in Claim 1 wherein said BPSG film has a thickness of not less than 50 nm but not greater than 200 nm.
3. A semiconductor device claimed in Claim 1 wherein a non-doped insulating film is formed between said diffusion layer and said interlayer insulating film.
4. A semiconductor device claimed in Claim 1 wherein said lower level wiring conductor layer also includes said polysilicon wiring conductor, and a non-doped insulating film is formed between said diffusion layer and said polysilicon wiring conductor and said interlayer insulating film.
5. A semiconductor device claimed in Claim 1 wherein said lower level wiring conductor layer includes a lower level wiring conductor formed of a refractory conductor material and said upper level wiring conductor formed of an aluminum type metal film.
6. A method for manufacturing a semiconductor device, comprising the steps:
 - forming a semiconductor device having a diffusion layer and a polysilicon wiring conductor at a silicon substrate surface, and forming a non-doped insulating film on a whole surface of the substrate;
 - forming, on said non-doped insulating film, a BPSG film having a thickness of not less than 50 nm but not greater than 200 nm, and then, performing a first heat-treatment;
 - forming, on said BPSG film, a non-doped silicon oxide film by a chemical vapor deposition process using ozone and tetraethoxysilane, and then, performing a second heat-treatment;
 - forming an insulative dummy layer on a surface of said non-doped silicon oxide film, and then, performing an etching-back treatment until said insulative dummy layer is completely removed, so that a surface of said non-doped silicon oxide film is planarized;
 - forming openings through said BPSG film and said non-doped silicon oxide film so as to reach said diffusion layer and said polysilicon wiring conductor, respectively; and
 - forming an upper level wiring conductor

formed of an aluminum type metal film on said planarized non-doped silicon oxide film, in contact with said diffusion layer and said polysilicon wiring conductor through said openings, respectively.

5

7. A method claimed in Claim 6 wherein each of said first and second heat-treatments is performed at a temperature of not lower than 700 °C but not higher than 800 °C.

10

8. A method claimed in Claim 6 wherein after said etching-back treatment is completed, an insulating film having a planar upper surface in an as-deposited condition is formed on said planarized non-doped silicon oxide film, and said openings are formed through said BPSG film, said non-doped silicon oxide film and said insulating film so as to reach said diffusion layer and said polysilicon wiring conductor, respectively.

15

20

9. A method claimed in Claim 8 wherein said insulating film is formed by coating and baking an SOG film on said surface of said non-doped silicon oxide film or by forming a photoresist film on said surface of said non-doped silicon oxide film.

25

10. A method claimed in Claim 6 wherein after said non-doped insulating film is formed, an opening is formed in said non-doped insulating film, and a lower level wiring conductor layer composed of a conductor film containing a refractory metal is formed; and

30

35

wherein there are formed openings reaching said diffusion layer, said polysilicon wiring conductor and said lower level wiring conductor layer composed of said conductor film containing said refractory metal, respectively.

40

45

50

55

FIGURE 1A PRIOR ART

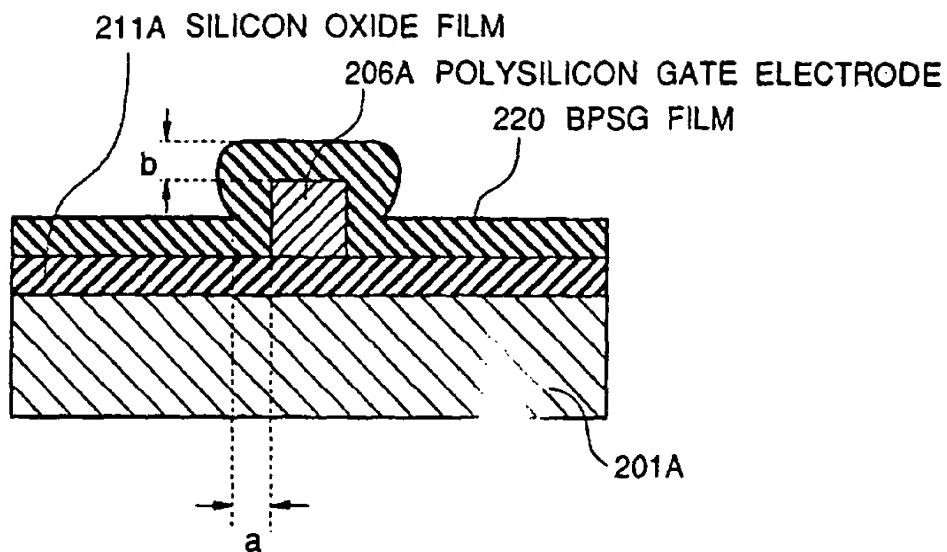


FIGURE 1B PRIOR ART

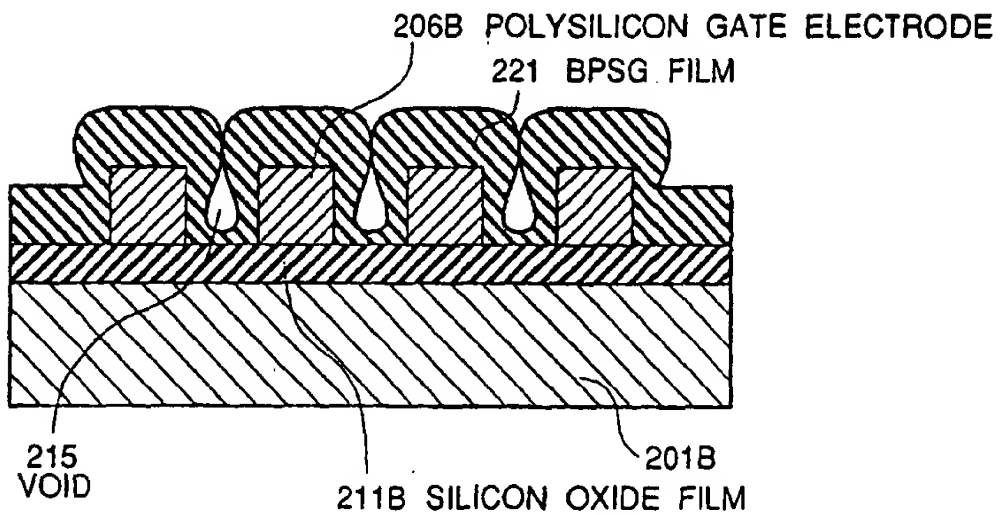


FIGURE 2 PRIOR ART

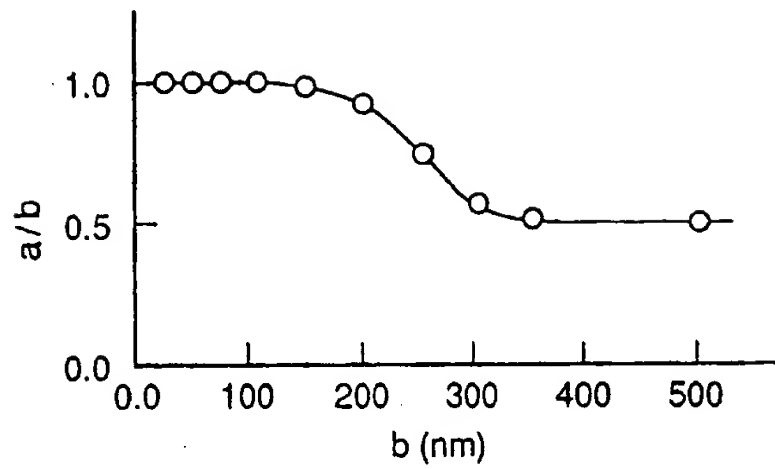


FIGURE 3A

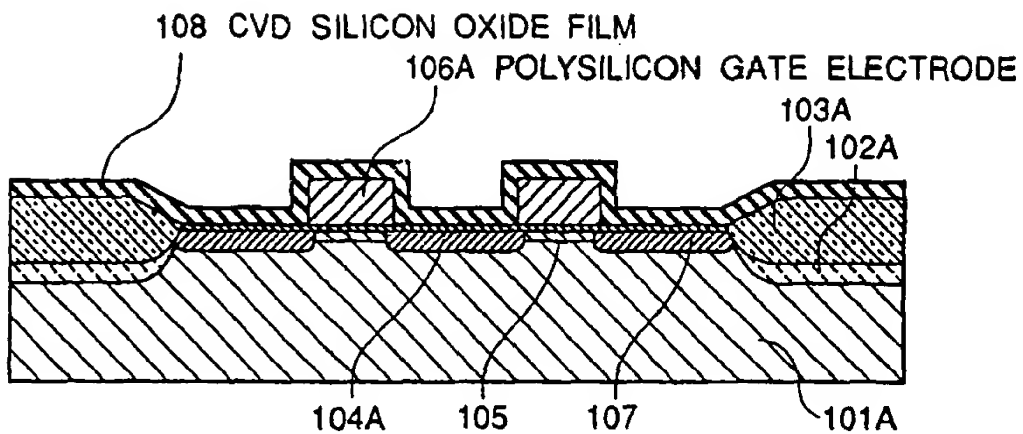


FIGURE 3B

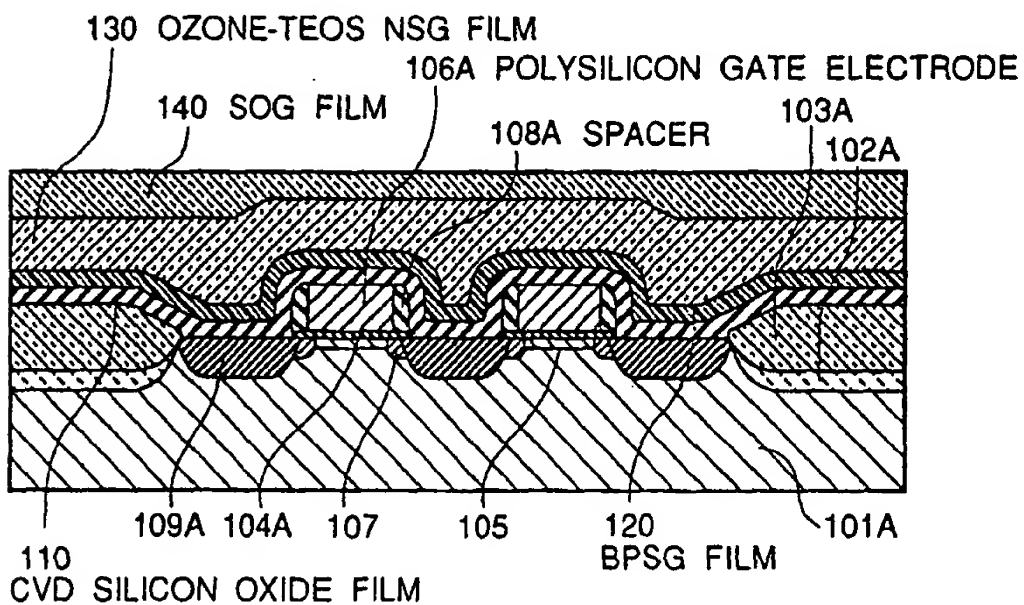


FIGURE 3C

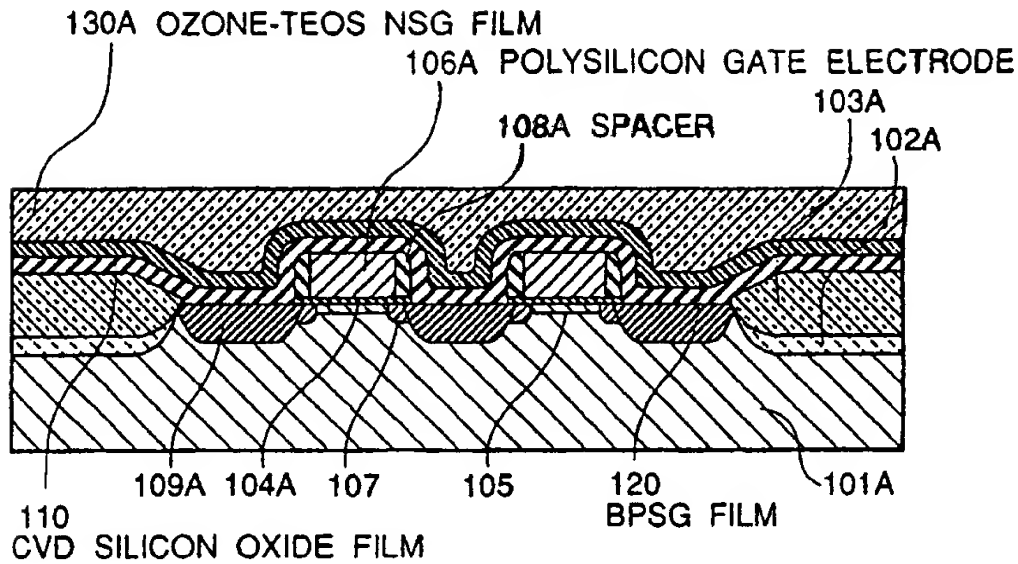


FIGURE 3D

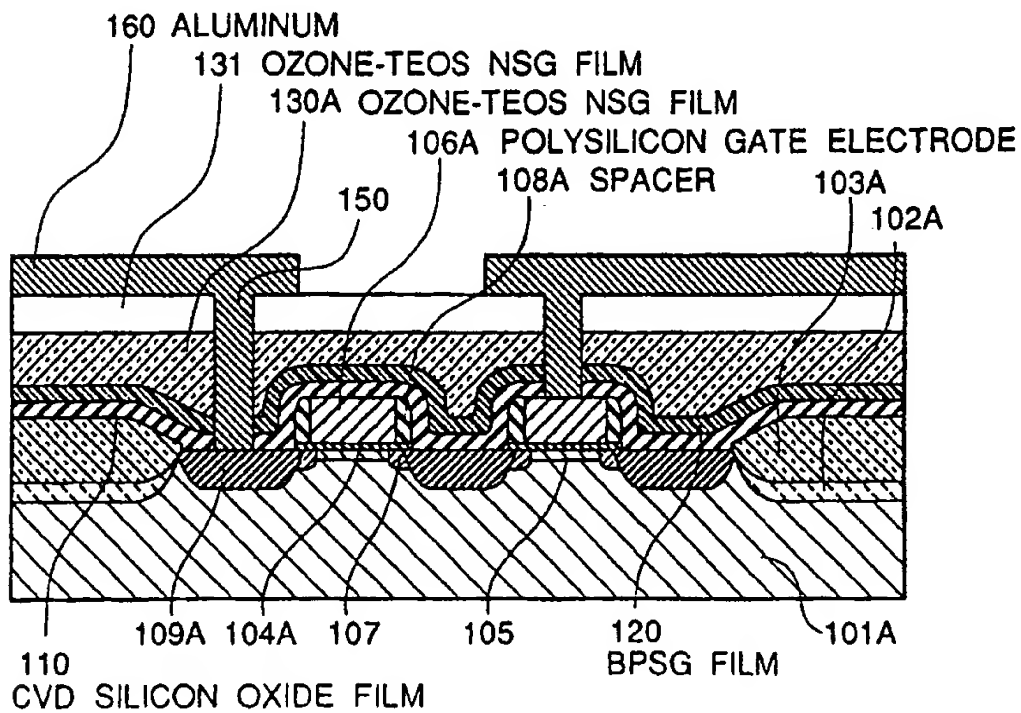


FIGURE 4A

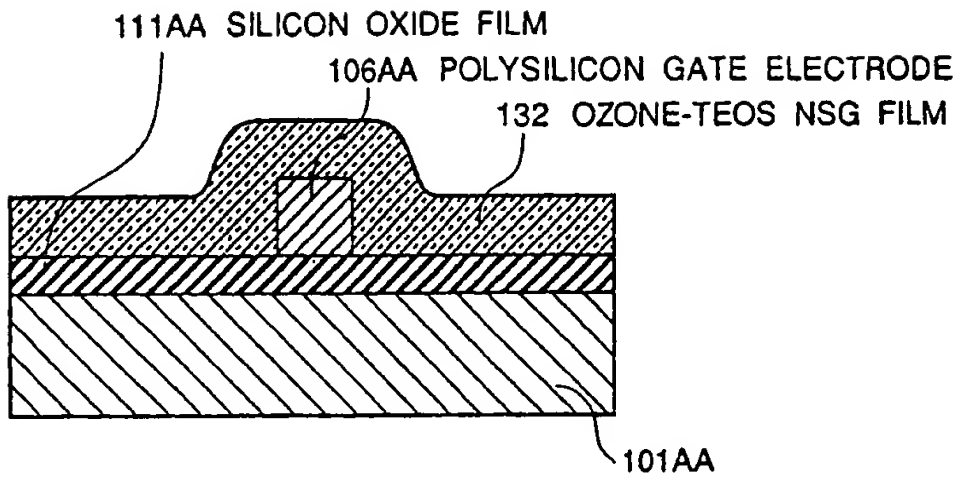


FIGURE 4B

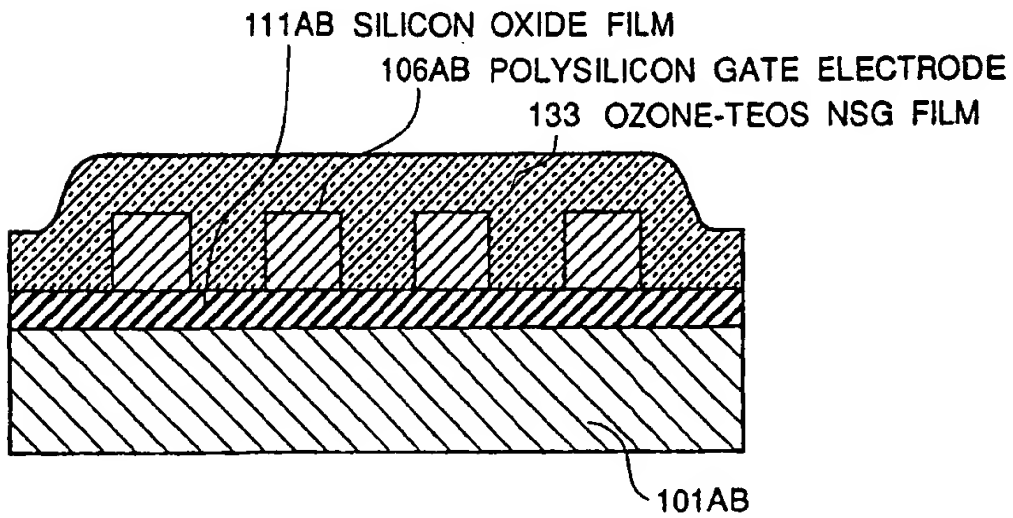


FIGURE 5

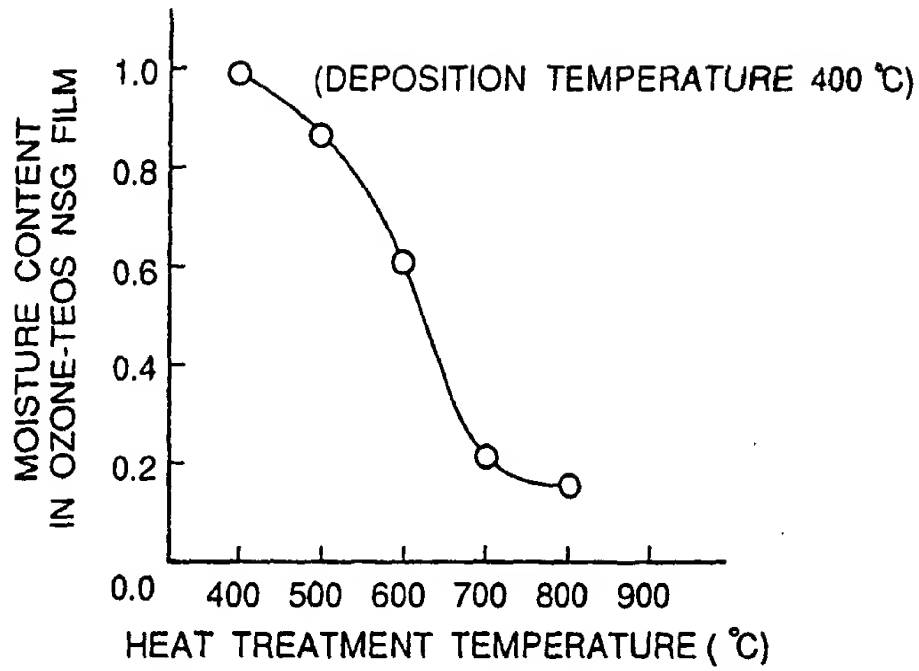


FIGURE 6

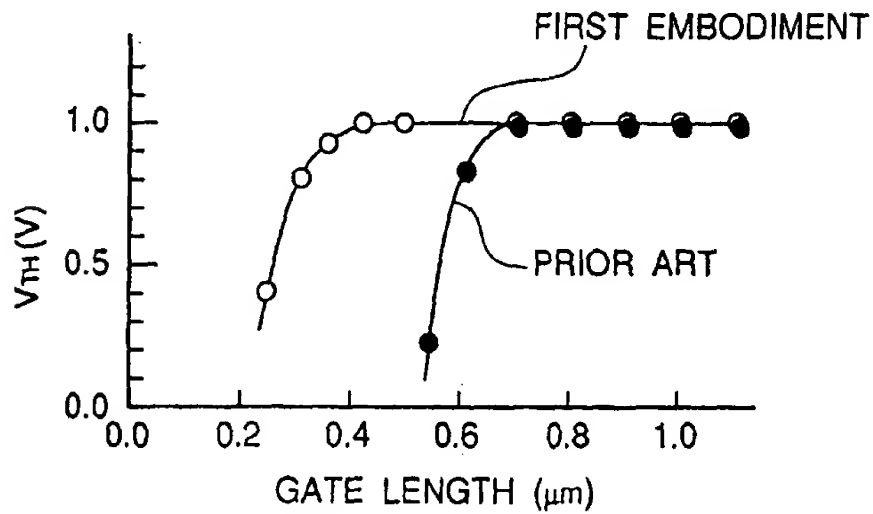
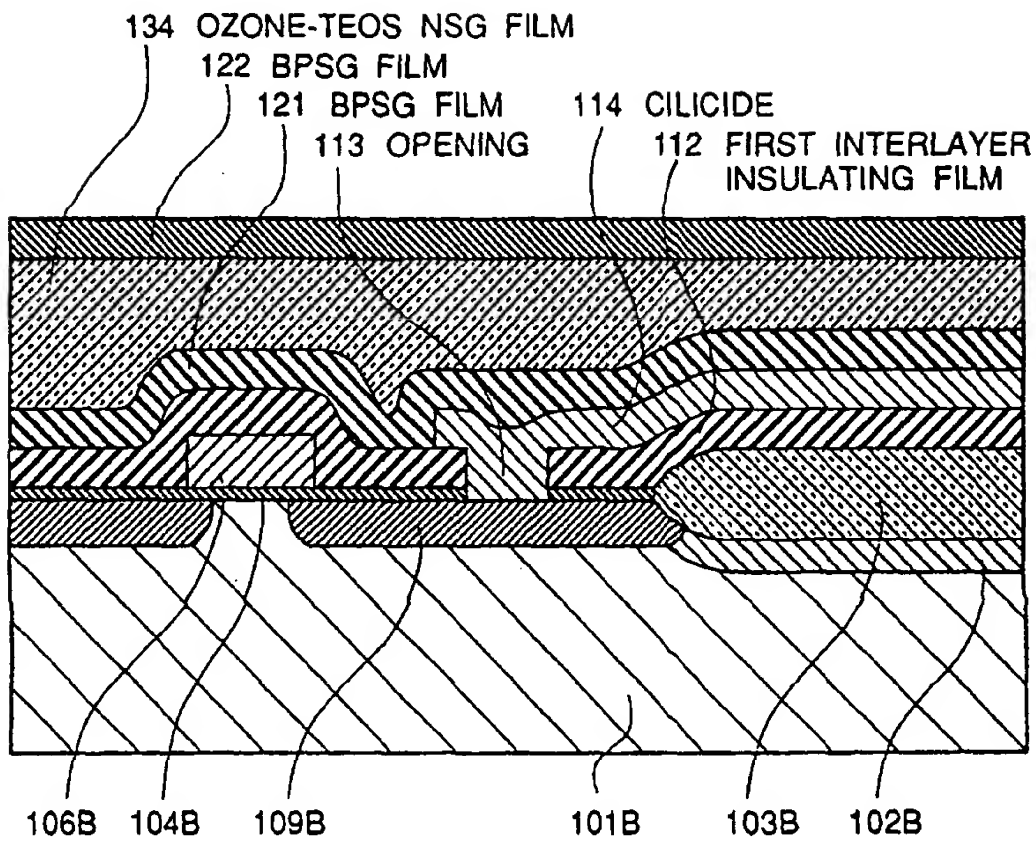


FIGURE 7





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 11 9027

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
P,X	EP-A-0 537 364 (SEMICONDUCTOR PROCESS LABORATORY CO., LTD.) * column 12, line 22 - column 16, line 46 * * figures 7-8 *	1,2,4	H01L21/90 H01L21/3105
A		5-7	
X	& WO-A-92 19011 (SEMICONDUCTOR PROCESS LABORATORY CO., LTD.) ---	1,2,4	
A	DE-A-41 00 525 (MITSUBISHI DENKI K., K.) * column 6, line 61 - column 7, line 22 * * figures 5A-5B * * figure 12 * * claims 1,13-19 *	1-4,6,10	
A	US-A-4 795 722 (M.T.WELCH ET AL.) * column 5, line 6 - column 6, line 45 * * figures 3-6 *	6,10	
A	EP-A-0 249 173 (ROCKWELL INTERNATIONAL CORP.) * column 8, line 18 - line 35 * -----	8	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			H01L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 1 March 1994	Examiner Schuermans, N
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

